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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application of:

Keeth et al.

Serial No.: 08/530,661

Filed: September 20, 1995

For: SEMICONDUCTOR MEMORY
CIRCUITRY

Examiner: D. Wille

Group Art Unit: 2814

Attorney Docket No.: 2269-5990US
(95-0424.00/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 6, 2003
Date

Rachael M. Harris
Signature

Rachel M. Harris
Name (Type/Print)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

| <u>U.S. Patent No.</u> | <u>Publication Date</u> | <u>Patentee</u> |
|------------------------|-------------------------|-----------------------|
| 5,013,680 | 05/07/91 | Lowrey et al. |
| 5,055,898 | 10/08/91 | Beilstein, Jr. et al. |
| 5,107,459 | 04/21/92 | Chu et al. |
| 5,396,450 | 03/07/95 | Takashima et al. |
| 5,555,519 | 09/10/96 | Takashima et al. |

Other Documents

European Search Report completed 26 February 2003 for European Application No. EP 03,001,319.

Asakura, M., "An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme," 29(11) IEEE Journal of Solid-State Circuits 1303-09 (Nov. 1994).

Denboer, Anthony, "Inside Today's Leading Edge Microprocessors," Semiconductor International (Feb. 1994).

Hamamoto, T., et al., "NAND-Structured Trench Capacitor Cell Technologies for 256 MB DRAM and Beyond," IEICE Transactions on Electronics, Institute of Electronics Information and Comm. Eng. Tokyo, JP, Vol. E78-C, NR. 7, pp. 789-796 (July 1995).

Sunouchi, K., et al., "A Surrounding Gate Transistor (SGT) cell for 64/256 Mbit DRAMs," EEDM 89 23 (1989), IEEE Inc., New York NY, pp. 2.1.1-2.1.4.

Watanabe, S., et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGTs) for Ultra High Density DRAM's" 30(9) IEEE Journal of Solid-State Circuits 960-70 (September 1, 1995).

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the first Office Action on the merits.

Serial No. 08/530,661

The fee pursuant to 37 C.F.R. § 1.17(p) is enclosed.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "K. K. Johanson", with a long, sweeping horizontal flourish extending to the right.

Kevin K. Johanson

Registration No. 38,506

Attorney for Applicants

TRASKBRITT

P.O. Box 2550

Salt Lake City, Utah 84110-2550

Telephone: 801-532-1922

Date: August 6, 2003

KKJ/sls:rmh

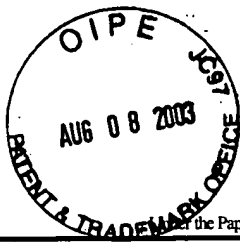
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PTO/SB/08B(10-01)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 2 of 2

Complete if Known

| | |
|------------------------|------------------------|
| Application Number | 08/530,661 |
| Filing Date | September 20, 1995 |
| First Named Inventor | Keeth et al. |
| Group Art Unit | 2814 |
| Examiner Name | D. Wille |
| Attorney Docket Number | 5990US (95-0424.00/US) |

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

| Examiner Initials * | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T ² |
|------------------------|--------------------------|---|----------------|
| | | European Search Report completed 26 February 2003 for European Application No. EP 03,001,319. | |
| | | Asakura, M., "An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme," 29(11) IEEE Journal of Solid-State Circuits 1303-09 (Nov. 1994). | |
| | | Denboer, Anthony, "Inside Today's Leading Edge Microprocessors," Semiconductor International (Feb. 1994). | |
| | | Hamamoto, T., et al., "NAND-Structured Trench Capacitor Cell Technologies for 256 MB DRAM and Beyond," IEICE Transactions on Electronics, Institute of Electronics Information and Comm. Eng. Tokyo, JP, Vol. E78-C, NR. 7, pp. 789-796 (July 1995). | |
| | | Sunouchi, K., et al., "A Surrounding Gate Transistor (SGT) cell for 64/256 Mbit DRAMs," EEDM 89 23 (1989), IEEE Inc., New York NY, pp. 2.1.1-2.1.4. | |
| | | Watanabe, S., et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGTs) for Ultra High Density DRAM's" 30(9) IEEE Journal of Solid-State Circuits 960-70 (September 1, 1995). | |
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Examiner
SignatureDate
Considered

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¹ Unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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